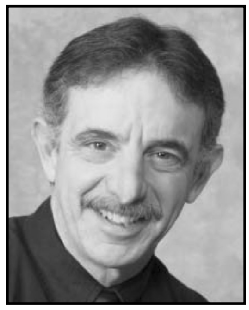
SE2 Circuit Design in the Year 2012



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Co-Organizer/Chair: Kerry Bernstein, IBM, Yorktown Heights, NY

The Technology Directions Subcommittee is pleased to present a special-topic-session format overview of special circuit design considerations which will accommodate sub-32nm device idiosyncrasies. While it is known that scaling effects will continue to profoundly impact high speed logic, designers rarely get a glimpse of the integrated response of all the resources on–board future high performance processors. Four forward-thinking experts will share their insight into issues confronting the microprocessor design team of 2012 and offer solutions we can begin to develop today to be ready.

David Frank begins our overview with an assessment of the impact of our technology scaling options on the design of microprocessors. Dr. Frank will first review alternative technology directions currently under study, and then assert their responses using a power-constrained optimization tool to anticipate their respective performance opportunities. The effect of enablements such as heatsinks, low-K dielectrics, and 3D integrations will be assessed.

The reduced signal swings and device gains associated with deeply-scaled future technologies present critical design problems for analog circuits, and will require substantial intervention and innovation. Our second speaker, Hae-Seung Lee, will review some of these challenges, which include leakage, flicker noise, and variability. Dr. Lee will explain how a new technique, “comparator-based switched capacitors”, may avoid many of the problems conventional analog circuits suffer from.

Given these heroic efforts to keep analog functions intact despite scaling effects, it is fair to ask whether the same criteria should be applied to the design of digital CMOS logic. Dr. Marcel Pelgrom will help answer the question of whether digital design should make the same tradeoffs in area vs. performance, reliability and system that analog designers chose. There are many problems and many opportunities, which include CAD tools, variability and finFETs.

FinFETs continue to be cited as potential scaling solutions for chips in 2012, given their superior electrostatics. Dr. Bora Nikolic will conclude our special topic session with an examination of the double-gated, fully-depleted MOSFET. Although finFET integration challenges such as thickness control and contact technology remain to be addressed, finFETs may arrive just in time to mitigate the substantial problems we have with SRAM stability.

Panelists Statements

Impact of Future Technology Scaling Options on Process Design
David Frank, IBM TJ Watson, Yorktown Heights, NY
A variety of technology options are being actively considered for the 32nm generation and beyond, including high-k gate dielectrics, metal gates, higher mobility channels, lower voltages, improved cooling technologies, and alternate FET geometries. In addition some unwanted effects will continue to increase in importance for these generations, including random variability and quantum mechanical effects such as band-to-band tunneling. These options and effects are summarized in this talk, and a power-constrained processor-oriented technology optimization tool is used to analyze their impact on overall chip performance. The power and temperature constraints significantly limit the effectiveness of many options. It is shown that high-k gate dielectrics offer significant advantage for PDSOI only if they are coupled with near-band-edge workfunction gates, and that performance only increases ~1% for every 10% increase in mobility. Improved heatsink technology can in principle allow significant performance improvement, but requires nearly exponential increses in the power dissipation. Lower dielectric constants for the wiring and 3D integration are also addressed.

Technology Scaling and Analog Circuits: Challenges and Solutions
Hae-Seung Lee, Massachusetts Institute of Technology, Cambridge, MA
Technology scaling has a significant impact on analog circuit design due to the reduced signal swing and the decreased intrinsic device gain. In addition, gate and subthreshold leakage currents, higher flicker noise corner frequency, and variations pose additional complications. In this paper, the difficulties imposed by technology scaling on analog circuits are examined, and possible solutions are proposed. In particular, a recent technique, the comparator based switched capacitor (CBSC) technique, has the potential to greatly outperform traditional analog circuits. Lack of explicit feedback and high device gain requirement, lower noise, and high power efficiency make CBSC circuits more suitable in scaled technologies. Traditional and CBSC analog circuits are compared on issues that arise from scaling down to 45nm. For numerical comparison, analog-to-digital converters in traditional and CBSC styles are contrasted in terms of projected figures-of-merit and absolute performance limits. Finally, some of the challenges designers may face in implementing high performance CBSC are discussed.

Digital Circuit Design Insights from Analog Experiences
Marcel Pelgrom, Phillips Research, Eindhoven, The Netherlands
The fundamental aspects of variability include phenomena such as threshold mismatch (often abbreviated to dopant fluctuation), line width variations etc. These local effects start to dominate the well-known global variations. In analog design a complete evolution of mitigation strategies has evolved: starting with auto-zero comparator, data weighted averaging and digital calibration(up to I/Q mixers). Is this an example for digital? Should the digital design community go the analog way and trade-off area versus extra transistors, data redundancy and system level solutions. What can and will be the role of a new set of CAD tools? Or wait for the finfets to solve the variability problems? This talk will review some of the problems in an analog/digital context and discuss the merits of various solutions.

Will FinFETs Replace Planar CMOS by Year 2012?
Borivoje Nikolic, University of California, Berkeley, CA
Vertical double-gate fully-depleted SOI transistors (finFETs) have intrinsically better electrostatics than the planar CMOS devices and present an opportunity for extended technology scaling. When competing with mainstream CMOS logic devices, the finFETs have to overcome the integration challenges, such as body thickness control, fin contacts, and mobility enhancements. On the other hand, planar CMOS 6-T SRAM faces significant stability challenges in scaling to 32-nm technology. The use of two independent gates allows for the design of stable 6-device finFET SRAM in sub-32nm processes. A technology that efficiently integrates in the same process the double-gate SRAM with planar CMOS logic could emerge by 2012.